FUDAN MICROELECTRONICS



FM4428 8KBits Memory Card Chip

Specification

May. 2008



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Specification 2

Product Overview

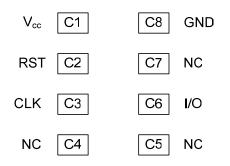
Description

FM4428 is the memory card chip developed by Shanghai FM Co, Ltd.. This chip uses 0.6µm CMOS EEPROM process, has 1K × 8Bit EEPROM with write protect function and programmable security code, its contact configuration is in accordance to ISO standard 7816 (Synchronous Transmission), FM4428 can be widely used in different types of IC memory cards.

Features

- 1024×8 bit EEPROM organization
- Byte-wise addressing
- Irreversible byte-wise write protection
- 1024×1 bit protection memory organization
- Serial three wire bus
- Minimum of 100,000 write/erase cycles
- Data retention for at least 10 years

Pin Configurations



Pin Functions

| PIN | Symbol | Function |
|-----|-----------------|-----------------------|
| C1 | V _{CC} | Operation voltage 5V |
| C2 | RST | Reset control |
| C3 | CLK | Clock |
| C4 | N.C. | Not connected |
| C5 | GND | Ground |
| C6 | N.C. | Not connected |
| C7 | I/O | Data line (pen drain) |
| C8 | N.C. | Not connected |

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- Contact configuration and serial interface in accordance to ISO standard 7816 (synchronous Transmission)
- Only after entry of the correct 2Byte programmable security code (PSC) data can be changed
- Compatible with SLE4428





Block Diagram

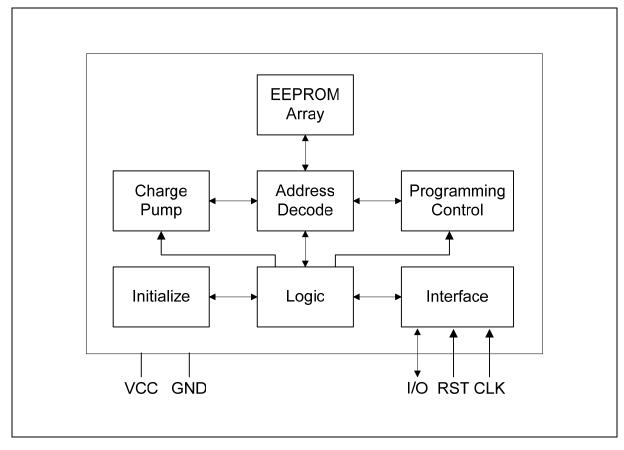


Figure 1-1 FM4428 Block Diagram

Function Description

Command Format

The chip receives input and gives output through I/O; the state of RST defines the data direction on I/O:

RST=1, I/O is for command entry

RST=0, I/O is for data output

Command takes the following format:

| b | B2 | b3 | b4 | b5 | b6 | b7 | b8 | b1 | B2 | b3 | b4 | b5 | b6 | b7 | b8 | b1 | b2 | b3 | b4 | b5 | b6 | b7 | b8 |
|---|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| S |) S1 | S2 | S3 | S4 | S5 | A8 | A9 | A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 |

Command is 24bit in length, organized in 3 Byte:

S0~S5 in byte 1 is control word for the command. The remaining 2 bits in byte 1 and the whole byte 2 add up 10 bits, they are address bit A0~A9. The last byte is for data bits D0-D7, in commands carrying out reading operations, this byte is of no effect.

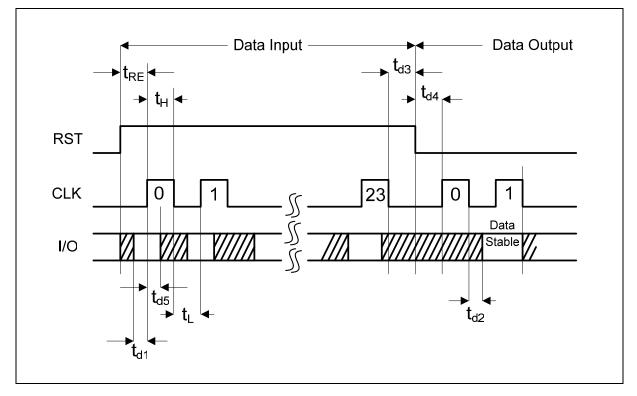


Figure 2-1 FM4428 General Timing Relationship

Command Introduction

(1) Erase/Write Data Byte with Protect Bit

| s0 | s1 | s2 | s3 | s4 | s5 | A8 A9 | A0-A7 | D0-D7 |
|----|----|----|----|----|----|---------------------|---------------------|------------|
| 1 | 0 | 0 | 0 | 1 | 1 | Address bit 8 and 9 | Address bit 0 and 7 | Input data |

The protect bit is enabled when data are written, memory area is set read only.

(2) Erase/Write Data Byte without Protect Bit

| s0 | s1 | s2 | s3 | s4 | s5 | A8 A9 | A0-A7 | D0-D7 |
|----|----|----|----|----|----|---------------------|---------------------|------------|
| 1 | 1 | 0 | 0 | 1 | 1 | Address bit 8 and 9 | Address bit 0 and 7 | Input data |

The protect bit is not enabled when data are written; memory area is still writable/erasable.

(3) Write Protect Bit with Date Comparison

| s0 | s1 | s2 | s3 | s4 | s5 | A8 A9 | A0-A7 | D0-D7 |
|----|----|----|----|----|----|---------------------|---------------------|-----------------|
| 0 | 0 | 0 | 0 | 1 | 1 | Address bit 8 and 9 | Address bit 0 and 7 | Comparison data |

When this command is carried out, the comparison data is compared with the contents in destination memory unit. If they are identical, then the corresponding protect bit is written as"0", otherwise, no change.

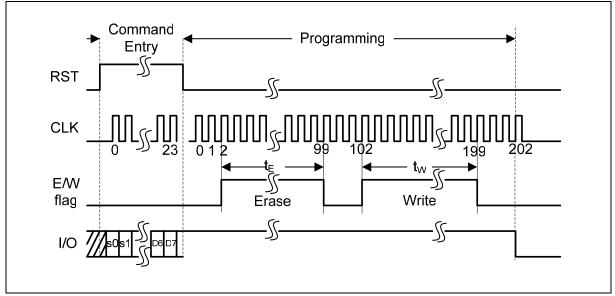


Figure 2-2 FM4428 Erase and Write

(If the operation is erase only, there is no WRITE part shown in the figure, hence lasting 102 CLK)

(4) Read Data Byte with Protect Bit

| s0 | s1 | s2 | s3 | s4 | s5 | A8 A9 | A0-A7 | D0-D7 |
|----|----|----|----|----|----|---------------------|---------------------|-----------|
| 0 | 0 | 1 | 1 | 0 | 0 | Address bit 8 and 9 | Address bit 0 and 7 | No effect |

This command reads out 8 data bits in destination address and the corresponding protect bit, adding up to 9 bit.

(5) Read Data Byte without Protect Bit

| s0 | s1 | s2 | s3 | s4 | s5 | A8 A9 | A0-A7 | D0-D7 |
|----|----|----|----|----|----|---------------------|---------------------|-----------|
| 0 | 1 | 1 | 1 | 0 | 0 | Address bit 8 and 9 | Address bit 0 and 7 | No effect |

This command reads out 8 data bits in destination address.

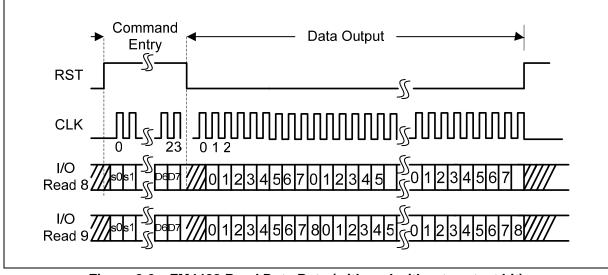


Figure 2-3 FM4428 Read Data Byte (with and without protect bit)

(6) Modify Error Counter

| s0 | s1 | s2 | s3 | s4 | s5 | A8 | A9 | A0-A7 | D0-D7 |
|----|----|----|----|----|----|----|----|-------|----------|
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 253 | Bit mask |

According to the entry mask word, change one bit "1" in the error counter to "0"

(7) Compare PSC Byte

| s0 | s1 | s2 | s3 | s4 | s5 | A8 | A9 | A0-A7 | D0-D7 |
|----|----|----|----|----|----|----|----|-----------|-------------------|
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 254 / 255 | PSC Byte 1/Byte 2 |

This command compares the entry PSC with contents stored in PSC memory area. After verification of comparison, erase operation can be carded out.

PSC Verification

The chip has a 2byte programmable security code (PSC). If failed to pass PSC verification, only reading is possible, while the contents of the PSC addresses cannot be read out. If failed to pass PSC verification, apart from writing to error counter bits, no other erase/write operation is allowed.

The verification procedure of the chip must be performed in the following steps:

- write one not written error-counter bit, address "1021";
- enter first PSC-code byte, address "1022";
- enter second PSC-code byte, address "1023";
- after correct input the error counter can be erased;

Whether PSC verification is passed can be judged from I/O state:

- 1). On the rising side of the 3rd lock after entry of the erase error counter command, if I/O state changes from "1" to "0", it means that PSC verification fails; error counter is unable to be erased.
- On the rising side of the 103rd clock after entry of the erase error counter command, if I/O state changes from "1" to "0", it means PSC verification passes, error counter has been written all "1".

Entry of PSC must start with the least-significant PSC byte with the least significant bit, and then the most –significant one. If PSC verification passes, all the memory is enabled for erasing and writing as long as operating voltage is applied, except those whose protect bit is "0". At this time, the error counter should be erased as all "1" in order to reactivate the next 8 attempts, The PSC may be altered as wished, if the corresponding protect bits are not effective.

Electrical Characteristics

Absolute Maximum Ratings

| Symbol | Parameter | Limit Values | | | | | |
|------------------|---------------------|--------------|-----|------|------|--|--|
| Symbol | Falameter | Min | Тур | Max | Unit | | |
| V _{CC} | Supply voltage | -0.3 | - | 6 | V | | |
| Vi | Input voltage | -0.3 | - | 6 | V | | |
| T _{sto} | Storage temperature | -40 | - | +125 | °C | | |
| P _{tot} | Power dissipation | - | - | 60 | mW | | |

DC Characteristics

| Symbol | Parameter | | Limit Values | 8 | unit |
|-----------------|---|-----|--------------|-----|------|
| Symbol | Falametei | Min | Тур | Max | um |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| I _{CC} | Supply current | - | 3 | 10 | mA |
| V _{ih} | H input voltage (I/O, CLK, RST) | 3.5 | - | Vcc | V |
| V _{il} | L input voltage (I/O, CLK, RST) | 0 | - | 0.8 | V |
| l _h | H input current (I/O, CLK, RST) | - | 3.9 | 10 | μA |
| I _{ol} | L input current (VI=0.4V, open drain) | 0.5 | - | - | mA |
| I _{oh} | H leakage current (VI=V _{cc} , open drain) | - | - | 10 | μA |
| Ci | Input capacitance | - | - | 10 | pF |
| F | Clock frequency | _ | 20 | - | kHz |
| Т | Test pin | 0 | pen or on GN | ND | |

AC Characteristics

| Symbol | Parameter | | Limit ValUe | 5 | unit |
|-----------------|---------------------------|-----|-------------|-----|------|
| Symbol | Falameter | Min | Тур | Max | um |
| t _{RE} | Reset time | 9 | - | - | μs |
| t _H | CLK (count, H level) | 10 | - | - | μs |
| tL | CLK (count, L level) | 10 | - | - | μs |
| t _{vv} | Write time | 5 | - | - | ms |
| t _E | Erase time | 5 | - | - | ms |
| t _{d1} | Setup time (D/CLK) | 4 | - | - | μs |
| t _{d3} | Setup time (CLK/RST) | 4 | - | - | μs |
| t _{d4} | Setup time (RST/CLK) | 4 | - | - | μs |
| t _{d5} | Hold time (D/CLK) | 4 | - | - | μs |
| t _{d2} | Delay time (CLK/D) | 6 | - | - | μs |
| t _R | Rise time (I/O, CLK, RST) | - | - | 1 | μs |
| t _F | Fall time (I/O, CLK, RST) | - | - | 1 | μs |

Revision History

| Version | Publication date | Pages | Paragraph or Illustration | Revise Description |
|---------|------------------|-------|------------------------------|---------------------------------------|
| 1.0 | Jun. 2001 | 6 | | Initial Release |
| 2.0 | Oct. 2007 | 11 | | Updated Format |
| 2.1 | May. 2008 | 11 | Sales and service | Updated the address of the HK office. |



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