

SLE 66R35E7

Intelligent 1 kByte Memory Chip
with Mifare compatibility and
7-byte Unique IDentification number

Short Product Information

2012-02-29
Preliminary

Edition 2012-02-29

**Published by
Infineon Technologies AG
81726 Munich, Germany**

**© 2012 Infineon Technologies AG
All Rights Reserved.**

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

SLE 66R35E7 - Short Product Information

Revision History: Current Version 2012-02-29

Previous Release: 2011-08-09

Page	Subjects (changes since last revision)
All	Editorial changes
10	Added information about personalization options (Table 4-2)
11	Corrected description of state transitions (Figure 4-3)

Trademarks of Infineon Technologies AG

AURIX™, BlueMoon™, C166™, CanPAK™, CIPOS™, CIPURSE™, COMNEON™, EconoPACK™, CoolMOS™, CoolSET™, CORECONTROL™, CROSSAVE™, DAVE™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPIM™, EiceDRIVER™, eupec™, FCOS™, HITFET™, HybridPACK™, I²RF™, ISOFACE™, IsoPACK™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OmniTune™, OptiMOS™, ORIGA™, PRIMARION™, PrimePACK™, PrimeSTACK™, PRO-SIL™, PROFET™, RASIC™, ReverSave™, SatRIC™, SIEGET™, SINDRION™, SIPMOS™, SMARTi™, SmartLEWIS™, SOLID FLASH™, TEMPFET™, thinQ!™, TRENCHSTOP™, TriCore™, X-GOLD™, X-PMU™, XMM™, XPOSYS™.

Other Trademarks

Advance Design System™ (ADS) of Agilent Technologies, AMBA™, ARM™, MULTI-ICE™, KEIL™, PRIMECELL™, REALVIEW™, THUMB™, μVision™ of ARM Limited, UK. AUTOSAR™ is licensed by AUTOSAR development partnership. Bluetooth™ of Bluetooth SIG Inc. CAT-iq™ of DECT Forum. COLOSSUS™, FirstGPS™ of Trimble Navigation Ltd. EMV™ of EMVCo, LLC (Visa Holdings Inc.). EPCOS™ of Epcos AG. FLEXGO™ of Microsoft Corporation. FlexRay™ is licensed by FlexRay Consortium. HYPERTERMINAL™ of Hilgraeve Incorporated. IEC™ of Commission Electrotechnique Internationale. IrDA™ of Infrared Data Association Corporation. ISO™ of INTERNATIONAL ORGANIZATION FOR STANDARDIZATION. MATLAB™ of MathWorks, Inc. MAXIM™ of Maxim Integrated Products, Inc. MICROTEC™, NUCLEUS™ of Mentor Graphics Corporation. MIPI™ of MIPI Alliance, Inc. MIPS™ of MIPS Technologies, Inc., USA. muRata™ of MURATA MANUFACTURING CO., MICROWAVE OFFICE™ (MWO) of Applied Wave Research Inc., OmniVision™ of OmniVision Technologies, Inc. Openwave™ Openwave Systems Inc. RED HAT™ Red Hat, Inc. RFMD™ RF Micro Devices, Inc. SIRIUS™ of Sirius Satellite Radio Inc. SOLARIS™ of Sun Microsystems, Inc. SPANSION™ of Spansion LLC Ltd. Symbian™ of Symbian Software Limited. TAIYO YUDEN™ of Taiyo Yuden Co. TEAKLITE™ of CEVA, Inc. TEKTRONIX™ of Tektronix Inc. TOKO™ of TOKO KABUSHIKI KAISHA TA. UNIX™ of X/Open Company Limited. VERILOG™, PALLADIUM™ of Cadence Design Systems, Inc. VLYNQ™ of Texas Instruments Incorporated. VXWORKS™, WIND RIVER™ of WIND RIVER SYSTEMS, INC. ZETEX™ of Diodes Zetex Limited.

Last Trademarks Update 2010-10-26

Remark:

Mifare is only used as an indicator of product compatibility to the respective technology.

Important:

For further information please contact:

Infineon Technologies AG in Munich, Germany,

Chip Card & Security

Fax: +49 (0)89 / 234-955 9372

E-Mail: security.chipcard.ics@infineon.com

Features

Intelligent 1 kByte Memory Chip with Mifare compatibility and 7-byte Unique IDentification Number

Contactless Interface

- Physical Interface and Anticollision compliant to ISO/IEC14443-2 and -3 Type A
 - Operation frequency 13.56 MHz; data rate 106 kbit/s
 - Contactless transmission of data and supply energy
 - Anticollision logic: several cards may be operated in the field simultaneously
 - Features Short-Cut Anticollision scheme to realize backward compatibility to installed infrastructures supporting 4-byte single size UIDs only
- Read and Write Distance up to 10 cm and more (influenced by external circuitry i.e. reader and inlay design)
- Short transaction times: typical ticketing transaction < 100 ms; transaction possible when card is moving

1 kByte EEPROM

- Block organization of memory, 16 Sectors with fixed 4 blocks of 16 bytes each
- EEPROM updating time per block < 4 ms
- Endurance > 100.000 erase/write cycles¹⁾
- Data Retention > 10 years¹⁾
- User definable access conditions for each memory block

Security Features

- 7-byte Unique IDentifier (UID) according to ISO/IEC 14443-3 Type A
- Support of 4-byte Random Number (RND-ID) and 4-byte fixed non-unique number (FNUID) according to ISO/IEC 14443-3 Type A
- Mutual three-pass authentication between card and reader for basic security
 - 48-bit key length
 - 2 keys per sector enabling key management
 - Transport key at chip delivery
- Selective memory access control secured by authentication and access conditions
- Suited to multifunctional applications: Individual key sets are available for each EEPROM sector
- Data encryption for RF channel
- Dedicated Value Counter
- Data integrity supported by CRC, Parity Check, etc.

Electrical characteristics

- On-chip capacitance 18.3 pF $\pm$ 10 %
- ESD protection typical 2 kV
- Ambient temperature -25 ... +70°C for the chip

1) Values are temperature dependent

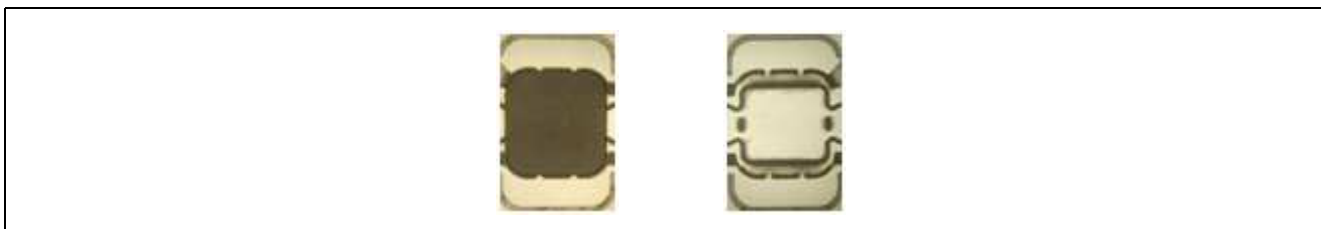
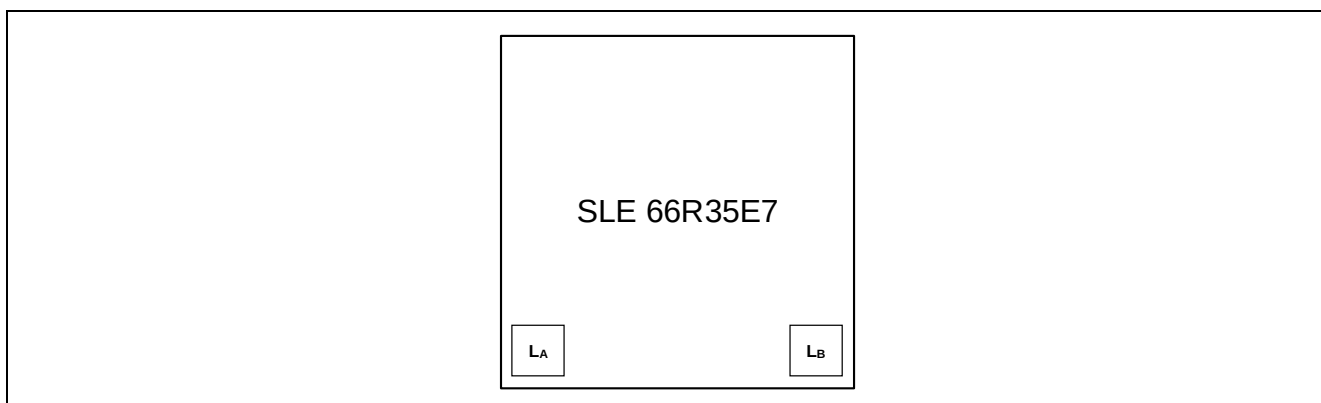
1 Ordering and Packaging Information

Table 1-1 Ordering information

Type	Package ¹⁾	Remark	Ordering code
SLE 66R35E7 C	Die (on wafer)	sawn / unsawn	on request
SLE 66R35E7 NB	Die (on wafer)	NiAu-bumps, sawn	on request
SLE 66R35E7 MCC2	MCC2-2-1		SP000981148
SLE 66R35E7 MCC8	MCC8-2-6		SP000981152

1) Available as a Module Contactless Card (MCC) for embedding in plastic cards, as NiAu-bumped version (NB) or as a die on sawn / unsawn wafer for customer packaging.

For more ordering information (wafer thickness or height of NiAu-bump) please contact your local Infineon sales office.


Figure 1-1 Pin Configuration Module Contactless Card - MCC2-2-1 (top view)

Figure 1-2 Pin Configuration Module Contactless Card - MCC8-2-6 (top / bottom view)

Figure 1-3 Pad Configuration Die
Table 1-2 Pin description and function

Symbol	Function
L _A	Antenna Connection
L _B	Antenna Connection

2 Overview of a Mifare compatible system

The SLE 66R35E7 is designed to operate in a Mifare compatible system. The system consists of a smart card and a card reader together with an antenna.

The operating distance between card and reader antenna is up to 10 cm and more (influenced by external circuitry i.e. reader-antenna configuration). The card's antenna consists of a simple coil with a few turns embedded in plastic.

The RF communication interface transmits at 106 kbit/s resulting in short transaction times, the effect being that a card user can move freely through a reader gate with minimum disruption. A typical ticketing transaction can be handled in less than 100 ms. Robust contactless transmission means that the card with SLE 66R35E7 may also remain in the wallet of the user even if there are coins in it.

An intelligent anticollision function based on the chip's double size unique identifier (uid0-uid6) enables more than one card in the field to operate simultaneously. The anticollision algorithm selects each card individually and enables the execution of a transaction with a selected card is performed correctly without data corruption resulting from other cards in the field.

The SLE 66R35E7 supports additional UID configurations allowing to operate SLE 66R35E7 in infrastructures running 4-byte (single cascade) anticollision schemes only (short-cut anticollision, Random Number, FNUID). Existing systems can remain unchanged. These options may be configured once during card personalization.

Access to SLE 66R35E7 is only allowed after a three-pass authentication. The serial number is unique for each card and cannot be changed. Each data transmission is enciphered. Protection from misuse is done by configurable access conditions that are protected by secret keys used for memory operations such as read or write.

Multi-Application Functionality

The SLE 66R35E7 is suited for the use in multi-application schemes, for example combining a transportation fare collection scheme and a ticketing system such as a stadium ticketing. Both applications can be performed with the same card, as hierarchical key management is supported. This means that two different keys for each memory sector can be assigned to enable authentication to that sector.

2.1 System Overview

The system consists of a host system, which is a contactless Read / Write Device connected to a background system, the antenna and one or more SLE 66R35E7 based tags or other ISO/IEC 14443-3 Type A compliant cards.

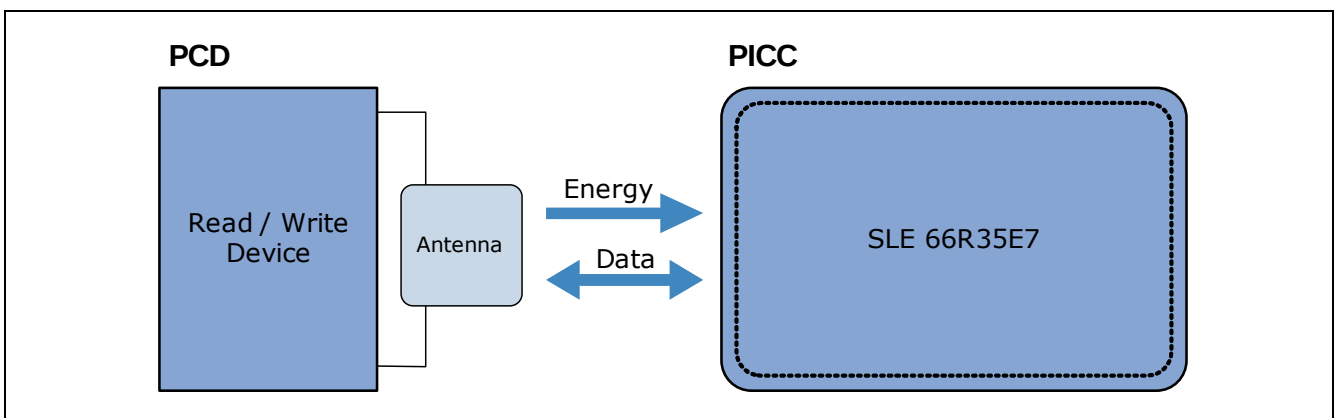


Figure 2-1 System Overview

2.2 Supported Standards

The SLE 66R35E7 supports the following standards:

- ISO/IEC 14443-1, -2 and -3 Type A
- Tested according to ISO/IEC 10373-6 (PICC Test & Validation)

2.3 Command Set

A set of standard ISO/IEC 14443-3 Type A commands is implemented to operate the chip.

Additionally the SLE 66R35E7 specific command set is implemented. This facilitates the access to the on-chip integrated memory, supports the execution of authentication, data de- and encryption as well as an increment or a decrement of a dedicated value counter.

3 Circuit Description

SLE 66R35E7 consists of an EEPROM memory of 1 kByte organized in 16 sector with 4 blocks each containing 16 bytes, an analog interface for contactless energy and data transmission and a control unit. The power supply and data are transferred to SLE 66R35E7 via an antenna, which consists of a coil with few turns directly connected to the module. No further external components are necessary. The circuit is designed to communicate with a card-reader at an operating distance of up to 10 cm (or more) depending on the reader-antenna configuration.

The chip is designed to meet the cost-optimized requirements of a basic security level. The targeted applications are transport, corporate access, events and loyalty cards with basic security requirements.

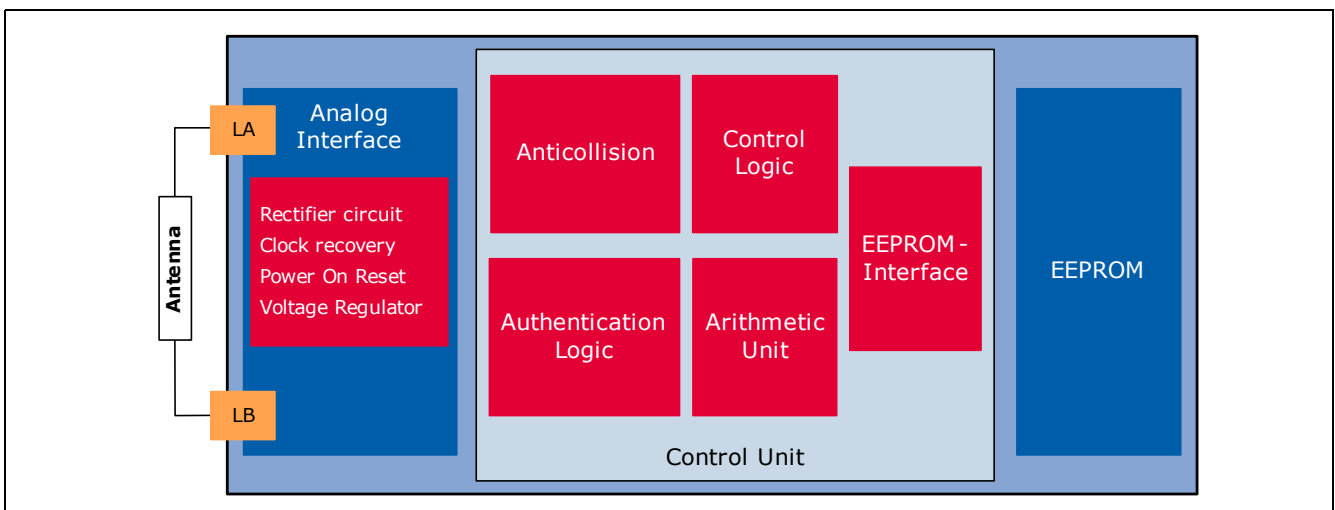


Figure 3-1 Block Diagram

- **Analog Contactless Interface:**
 - The Analog Contactless Interface comprises the voltage rectifier, voltage regulator and system clock to supply the IC with appropriate power. Additionally the data stream is modulated and demodulated.
- **Anticollision**
 - Internal logic of SLE 66R35E7 ensures the recognition of several cards in the field which may be selected and operated in sequence.
- **Authentication Logic**
 - Correct execution of any memory operation can only occur after the authentication procedure with a specific key.
- **Control Logic**
 - Access to a block is defined by the associated access conditions for that block. These are programmed individually for each block in a sector.
- **Arithmetic Unit**
 - Arithmetic Capability: increment and decrement of values stored in a special redundant format.
- **EEPROM:**
 - 1 kByte organized in 16 sectors with 4 blocks by 16 bytes each. The last block of each sector is called "Sector Trailer" and is used to store for a pair of secret keys and programmable access conditions for each block.

4 SLE 66R35E7 Options

SLE 66R35E7 supports systems based on single and double size UUIDs:

- 7-byte Unique Identifier (UID) according to ISO/IEC 14443-3 Type A
- 4-byte Random Number (RND-ID) according to ISO/IEC 14443-3 Type A
- 4-byte fixed non-unique number (FNUID) according to ISO/IEC 14443-3 Type A

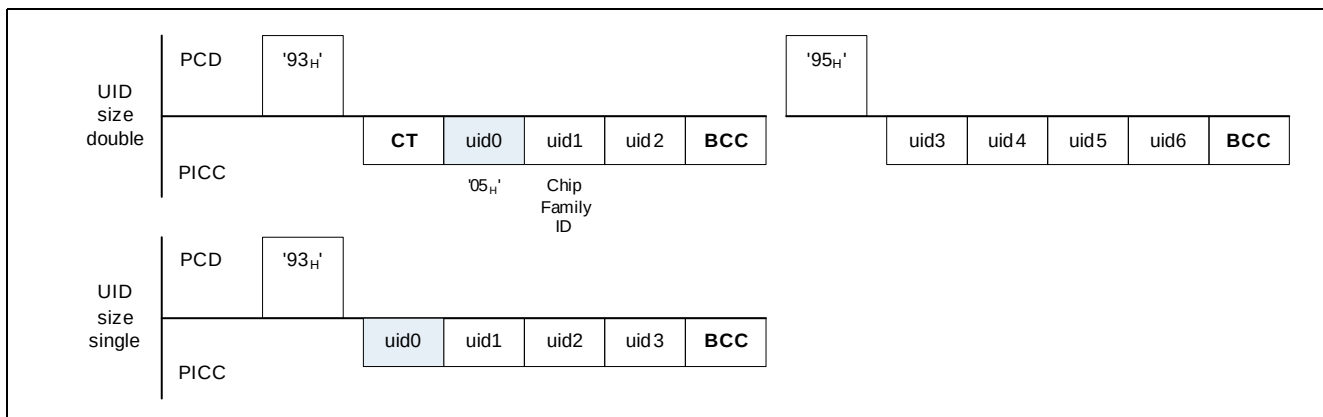


Figure 4-1 UUIDs according to ISO/IEC 14443-3 Type A

4.1 Product Overview

Following memory chips with Mifare compatibility are available:

Table 4-1 Overview on Chip Types using Mifare Technology

Type	UID size	UID type	uid0	Description
SLE 66R35 ¹⁾ 2)	4-byte	UID	xM _H P8 _H	Fixed unique number programmed by manufacturer (M = 1, 5, 7, 9) (P = 1, 2, 3, 4, 5)
SLE 66R35I	4-byte	FNUID	xF _H	Fixed number, non-unique programmed by manufacturer
SLE 66R35R	4-byte	r-ID	x1 _H	Fixed reused identity number programmed by manufacturer
SLE 66R35E7	7-byte	UID	05 _H	Fixed unique number programmed by manufacturer (delivery default)
	4-byte	FNUID	xF _H	Fixed number, non-unique derived from 7-byte UID (personalization option). The FNUID is not stored in Block 00 _H , it is derived from the 7-byte UID stored in Block 00 _H . The derived value for the uid0 byte is logically or-ed with 1F _H ; due to that x may have following values: 1 _H , 3 _H , 5 _H , 7 _H , 9 _H , B _H , D _H , F _H
	4-byte	RND-ID	08 _H	uid1 to uid3 is a random number (RND1 - RND3) (personalization option). The RND-ID is not stored in Block 00 _H ; a new RND-ID is generated with every power-up.

1) The available numbers are already exhausted.

2) Discontinued. Consider to use successor products SLE 66R35I, SLE 66R35R or SLE 66R36E7.

4.2 Personalization Options

SLE 66R35E7 can be configured during issuing of a card using the *CONFIGURE_UID* command.

Table 4-2 UID options

UID Option	Anticollision and selection
UIDF0	7-byte UID only (delivery default)
UIDF1	7-byte UID and optional usage of short-cut anticollision scheme
UIDF2	4-byte Random number (RND-ID) uid0 = 08 _H uid1 - uid3 = RND1 - RND3
UIDF3	4-byte Fixed number, non-unique ID (FNUID) uid0 = xF _H (x = 1, 3, 5, 7, 9, B, D, F)

4.3 SLE 66R35E7 - 7-byte UID Configuration

The SLE 66R35E7 is delivered as 7-byte UID device. Block 00_H is configured as shown in following figure:

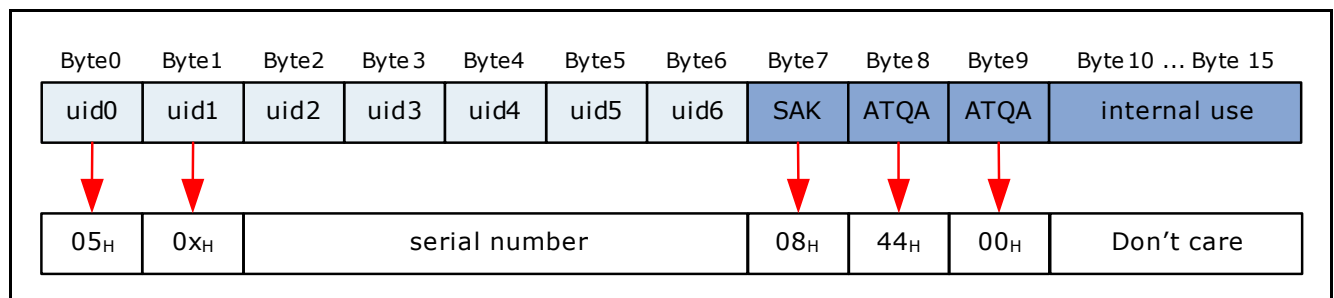


Figure 4-2 Memory Structure Block 00_H

- uid0 = 05_H identifies Infineon Technologies as chip manufacturer according to ISO/IEC 7816-6 standard
- uid1 holds information about the Chip Family

Table 4-3 Chip Family Identifier

uid1 coding ¹⁾	Chip Family	Description
0x _H	SLE 66R35E7	Mifare compatible product with 7-byte UID
1x _H	SLE 66RxxS	my-d™ proximity 2
2x _H	SLE 66RxxP	my-d™ NFC
3x _H	SLE 66R01P	my-d™ move
7x _H	SLE 66R01L	my-d™ move lean
All other		Please contact Infineon Technologies sales

1) 'x' is part of the serial number.

Please also refer to the application note "Anticollision and UID Options" for further information on UIDs as used for Infineon Products.

Anticollision for CL1 (Short-cut) and CL2

The SLE 66R35E7 supports the both anticollision schemes cascade level 1 (short-cut anticollision) and 2. The short-cut anticollision allows to operate the SLE 66R35E7 even in infrastructures with 4-byte (single cascade) anticollision scheme. Existing systems based on CL1 can remain unchanged.

If the Short-cut anticollision scheme has been enabled (UIDF1 Option, see [Chapter 4.2](#)) in READY2 / READY2* state the chip accepts:

- a READ (Block 00_H) command: the SLE 66R35E7 then executes a state transition to ACTIVE / ACTIVE* state. Following authentication commands will use the last four UID bytes sent to the PCD.
- an AUTHENTICATE command to a sector: the SLE 66R35E7 then executes a state transition to the AUTHx state applying the UID bytes used for cascade level 1 selection (SEL CL1).

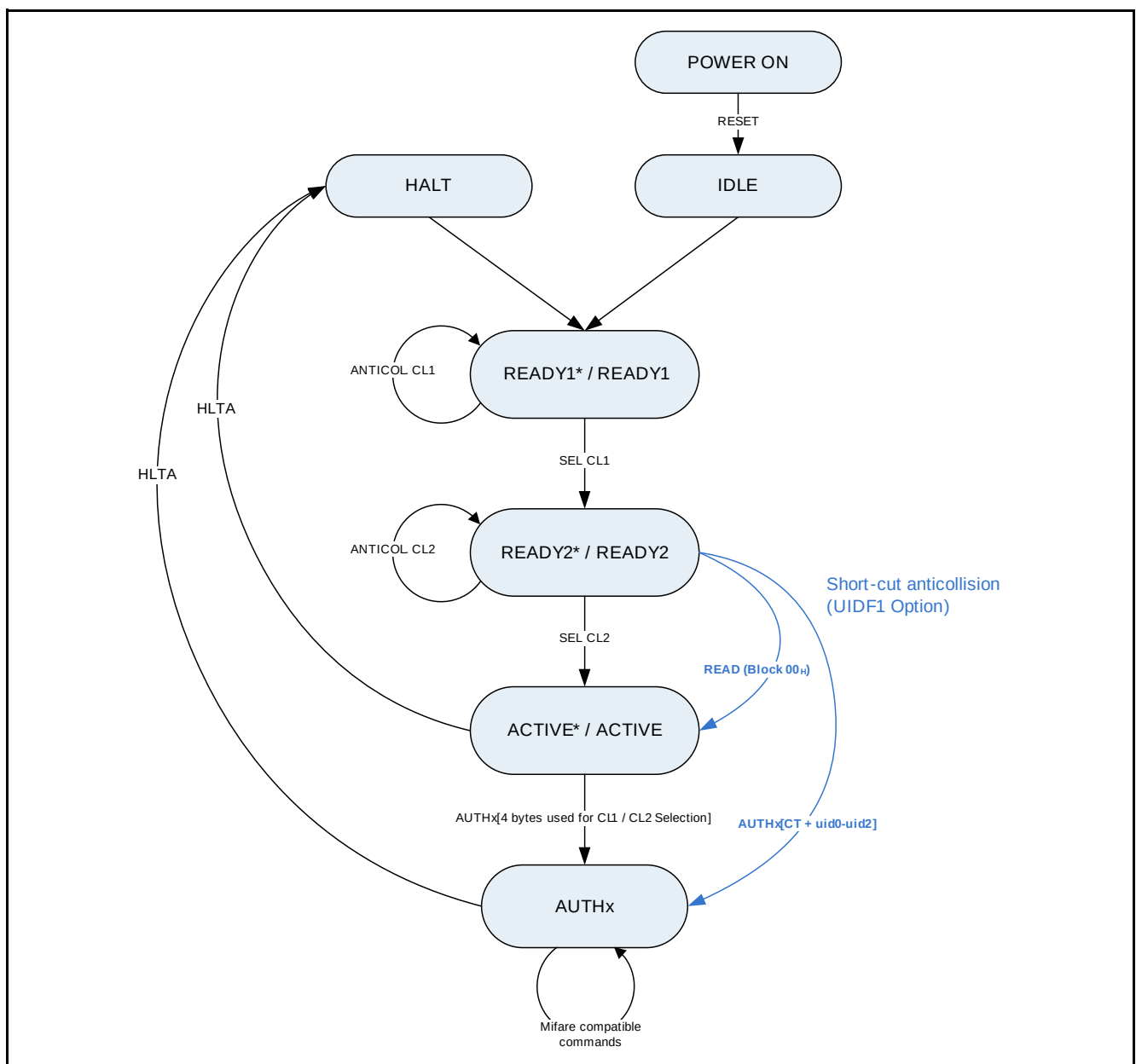


Figure 4-3 Anticollision for UIDF0 and UIDF1 Options

4.4 SLE 66R35E7 - 4-byte UID Configurations

The SLE 66R35E7 also supports single cascade anticollision schemes.

- 4-byte Random Number (RND-ID)
- 4-byte fixed non-unique number (FNUID)

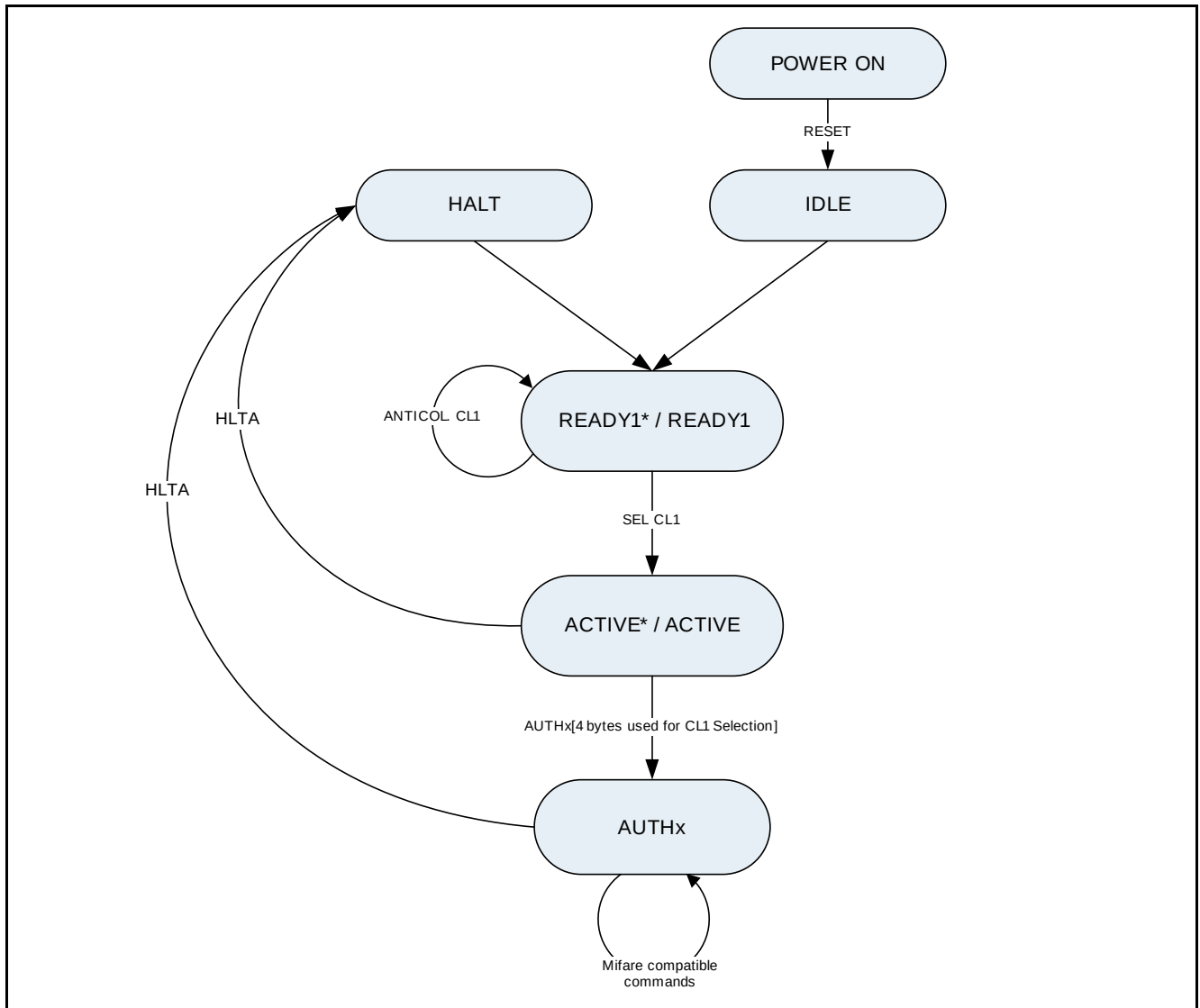


Figure 4-4 Anticollision for UIDF2 and UIDF3 Options

www.infineon.com